19-1295; Rev 4; 1/02

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps



## General Description

The MAX4249–MAX4257 low-noise, low-distortion operational amplifiers offer Rail-to-Rail® outputs and single-supply operation down to 2.4V. They draw 400µA of quiescent supply current per amplifier while featuring ultra-low distortion (0.0002% THD), as well as low input voltage-noise density (7.9nV/√Hz) and low input current-noise density (0.5fA/√Hz). These features make the devices an ideal choice for portable/battery-powered applications that require low distortion and/or low noise.

For additional power conservation, the MAX4249/MAX4251/MAX4253/MAX4256 offer a low-power shutdown mode that reduces supply current to 0.5µA and puts the amplifiers' outputs into a high-impedance state. The MAX4249-MAX4257's outputs swing rail-to-rail and their input common-mode voltage range includes ground. The MAX4250–MAX4254 are unity-gain stable with a gain-bandwidth product of 3MHz. The MAX4249/MAX4255/MAX4256/MAX4257 are internally compensated for gains of 10V/V or greater with a gain-bandwidth product of 22MHz. The single MAX4250/MAX4255 are available in space-saving 5-pin SOT23 packages. The MAX4252 is available in an 8-pin ultra chip-scale package (UCSP™) and the MAX4253 is available in a 10-pin UCSP.

## Applications

- Wireless Communications Devices
- PA Control
- Portable/Battery-Powered Equipment
- Medical Instrumentation
- ADC Buffers
- Digital Scales/Strain Gauges

## Features

- ♦ **Available in Space-Saving UCSP, SOT23, and µMAX Packages**
- ♦ **Low Distortion: 0.0002% THD (1kΩ load)**
- ♦ **400µA Quiescent Supply Current per Amplifier**
- ♦ **Single-Supply Operation from 2.4V to 5.5V**
- ♦ **Input Common-Mode Voltage Range Includes Ground**
- ♦ **Outputs Swing Within 8mV of Rails with a 10kΩ Load**
- ♦ **3MHz GBW Product, Unity-Gain Stable (MAX4250–MAX4254)**

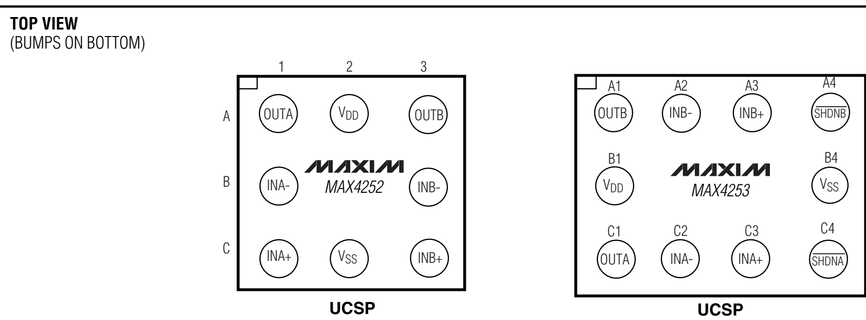
  **22MHz GBW Product, Stable with $A_V \geq$ 10V/V (MAX4249/MAX4255/MAX4256/MAX4257)**
- ♦ **Excellent DC Characteristics**
  - **$V_{OS}$ = 70µV**
  - **$I_{BIAS}$ = 1pA**
  - **Large-Signal Voltage Gain = 116dB**
- ♦ **Low-Power Shutdown Mode:**
  - **Reduces Supply Current to 0.5µA**
  - **Places Outputs in a High-Impedance State**
- ♦ **400pF Capacitive-Load Handling Capability**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|---|---|---|---|
| **MAX4249**ESD | -40°C to +85°C | 14 SO | — |
| MAX4249EUB | -40°C to +85°C | 10 µMAX | — |
| **MAX4250**EUK-T | -40°C to +85°C | 5 SOT23-5 | ACCI |

***Ordering Information continued at end of data sheet.***
***Selector Guide appears at end of data sheet.***

## Pin Configurations




*Pin Configurations continued at end of data sheet.*

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage ($V_{DD}$ to $V_{SS}$) .....................+6.0V to -0.3V
Analog Input Voltage (IN_+, IN_-)....($V_{DD}$ + 0.3V) to ($V_{SS}$ - 0.3V)
$\overline{SHDN}$ Input Voltage .....................................6.0V to ($V_{SS}$ - 0.3V)
Output Short-Circuit Duration to Either Supply ..........Continuous
Continuous Power Dissipation ($T_A$ = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C)...........571mW
8-Pin µMAX (derate 4.5mW/°C above +70°C) ...........362mW
8-Pin SO (derate 5.88mW/°C above +70°C)..............471mW
8-Pin UCSP (derate 4.7mW/°C above +70°C) ...........379mW
10-Pin UCSP (derate 6.1mW/°C above +70°C) ..........484mW
10-Pin µMAX (derate 5.6mW/°C above +70°C) ...........444mW
14-Pin SO (derate 8.33mW/°C above +70°C).............667mW
Operating Temperature Range ...........................-40°C to +85°C
Junction Temperature ......................................................+150°C
Storage Temperature Range ............................-65°C to +150°C
Lead Temperature (soldering, 10s) ................................+300°C
Bump Temperature (soldering) (Note 1)
Infrared (15s) ...............................................................+220°C
Vapor Phase (60s) .......................................................+215°C

**Note 1:** This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragrah 7.6, Table 3 for IR/VPR and Convection Reflow. Preheating is required. Hand or wave soldering is not allowed.

*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = 0, $V_{OUT}$ = $V_{DD}$/2, $R_L$ tied to $V_{DD}$/2, $\overline{SHDN}$ = $V_{DD}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage Range | $V_{DD}$ | (Note 4) | | 2.4 | | 5.5 | V |
| Quiescent Supply Current Per Amplifier | $I_Q$ | Normal mode | $V_{DD}$ = 3V | | 400 | | µA |
| | | | $V_{DD}$ = 5V | | 420 | 575 | |
| | | | $V_{DD}$ = 5V, UCSP only | | 420 | 655 | |
| | | Shutdown mode ($\overline{SHDN}$ = $V_{SS}$) (Note 2) | | | 0.5 | 1.5 | |
| Input Offset Voltage (Note 5) | $V_{OS}$ | | | | ±0.07 | ±0.75 | mV |
| Input Offset Voltage Tempco | $TCV_{OS}$ | | | | 0.3 | | µV/°C |
| Input Bias Current | $I_B$ | (Note 6) | | | ±1 | ±100 | pA |
| Input Offset Current | $I_{OS}$ | (Note 6) | | | ±1 | ±100 | pA |
| Differential Input Resistance | $R_{IN}$ | | | | 1000 | | GΩ |
| Input Common-Mode Voltage Range | $V_{CM}$ | Guaranteed by CMRR test | | -0.2 | | $V_{DD}$ - 1.1 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{SS}$ - 0.2V ≤ $V_{CM}$ ≤ $V_{DD}$ - 1.1V | | 70 | 115 | | dB |
| Power-Supply Rejection Ratio | PSRR | $V_{DD}$ = 2.4 to 5.5V | | 75 | 100 | | dB |
| Large-Signal Voltage Gain | $A_V$ | $R_L$ = 10kΩ to $V_{DD}$/2; $V_{OUT}$ = 25mV to $V_{DD}$ - 4.97V | | 80 | 116 | | dB |
| | | $R_L$ = 1kΩ to $V_{DD}$/2; $V_{OUT}$ = 150V to $V_{DD}$ - 4.75V | | 80 | 112 | | |
| Output Voltage Swing | $V_{OUT}$ | $\lvert V_{IN+} - V_{IN-} \rvert$ ≥ 10mV $R_L$ = 10kΩ to $V_{DD}$/2 | $V_{DD}$ - $V_{OH}$ | | 8 | 25 | mV |
| | | | $V_{OL}$ - $V_{SS}$ | | 7 | 20 | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = 0, $V_{OUT}$ = $V_{DD}$/2, $R_L$ tied to $V_{DD}$/2, $\overline{SHDN}$ = $V_{DD}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Voltage Swing | $V_{OUT}$ | $\lvert V_{IN+} - V_{IN-} \rvert \geq$ 10mV, $R_L$ = 1kΩ to $V_{DD}$/2 | $V_{DD}$ - $V_{OH}$ | | 77 | 200 | mV |
| | | | $V_{OL}$ - $V_{SS}$ | | 47 | 100 | |
| Output Short-Circuit Current | $I_{SC}$ | | | | 68 | | mA |
| Output Leakage Current | $I_{LEAK}$ | Shutdown mode ($\overline{SHDN}$ = $V_{SS}$), $V_{OUT}$ = $V_{SS}$ to $V_{DD}$ (Note 2) | | | 0.001 | 1.0 | µA |
| $\overline{SHDN}$ Logic Low | $V_{IL}$ | (Note 2) | | | | 0.2 x $V_{DD}$ | V |
| $\overline{SHDN}$ Logic High | $V_{IH}$ | (Note 2) | | 0.8 x $V_{DD}$ | | | V |
| $\overline{SHDN}$ Input Current | $I_{IL}/I_{IH}$ | $\overline{SHDN}$ = $V_{SS}$ = $V_{DD}$ (Note 2) | | | 0.5 | 1.5 | µA |
| Input Capacitance | | | | | 11 | | pF |
| Gain-Bandwidth Product | GBW | MAX4250–MAX4254 | | | 3 | | MHz |
| | | MAX4249/MAX4255/MAX4256/MAX4257 | | | 22 | | |
| Slew Rate | SR | MAX4250–MAX4254 | | | 0.3 | | V/µs |
| | | MAX4249/MAX4255/MAX4256/MAX4257 | | | 2.1 | | |
| Peak-to-Peak Input-Noise Voltage | $e_{nP-P}$ | f = 0.1Hz to 10Hz | | | 760 | | $nV_{P-P}$ |
| Input Voltage-Noise Density | $e_n$ | f = 10Hz | | | 2.7 | | nV/√Hz |
| | | f = 1kHz | | | 8.9 | | |
| | | f = 30kHz | | | 7.9 | | |
| Input Current-Noise Density | $i_n$ | f = 1kHz | | | 0.5 | | fA/√Hz |
| Total Harmonic Distortion Plus Noise | THD + N | MAX4250–MAX4254 $A_V$ = 1V/V, $V_{OUT}$ = $2V_{P-P}$, $R_L$ = 1kΩ to GND (Note 7) | f = 1kHz | | 0.0004 | | % |
| | | | f = 20kHz | | 0.006 | | |
| | | MAX4249/MAX4255/ MAX4256/MAX4257 $A_V$ = 1V/V, $V_{OUT}$ = $2V_{P-P}$, $R_L$ = 1kΩ to GND (Note 7) | f = 1kHz | | 0.0012 | | |
| | | | f = 20kHz | | 0.007 | | |
| Capacitive-Load Stability | | No sustained oscillations | | | 400 | | pF |
| Gain Margin | GM | MAX4250–MAX4254, $A_V$ = 1V/V | | | 10 | | dB |
| | | MAX4249/MAX4255/MAX4256/MAX4257, $A_V$ = 10V/V | | | 12.5 | | |
| Phase Margin | ΦM | MAX4250–MAX4254, $A_V$ = 1V/V | | | 74 | | degrees |
| | | MAX4249/MAX4255/MAX4256/MAX4257, $A_V$ = 10V/V | | | 68 | | |

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = 0, $V_{OUT}$ = $V_{DD}$/2, $R_L$ tied to $V_{DD}$/2, $\overline{SHDN}$ = $V_{DD}$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 3)

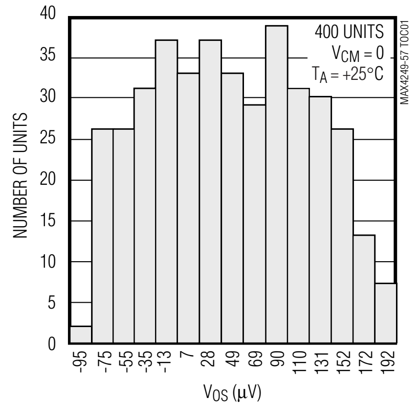
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Settling Time | | To 0.01%, $V_{OUT}$ = 2V step | MAX4250–MAX4254 | | 6.7 | | µs |
| | | | MAX4249/MAX4255/ MAX4256/MAX4257 | | 1.6 | | |
| Delay Time to Shutdown | $t_{SH}$ | $I_{VDD}$ = 5% of normal operation | MAX4251/MAX4253 | | 0.8 | | µs |
| | | | MAX4249/MAX4256 | | 1.2 | | |
| Delay Time to Enable | $t_{EN}$ | $V_{OUT}$ = 2.5V, $V_{OUT}$ settles to 0.1% | MAX4251/MAX4253 | | 8 | | µs |
| | | | MAX4249/MAX4256 | | 3.5 | | |
| Power-Up Delay Time | $t_{PU}$ | $V_{DD}$ = 0 to 5V step, $V_{OUT}$ stable to 0.1% | | | 6 | | µs |

**Note 2:** $\overline{SHDN}$ is available on the MAX4249/MAX4251/MAX4253/MAX4256 only.
**Note 3:** All device specifications are 100% tested at $T_A$ = +25°C. Limits over temperature are guaranteed by design.
**Note 4:** Guaranteed by the PSRR test.
**Note 5:** Offset voltage prior to reflow on the UCSP.
**Note 6:** Guaranteed by design.
**Note 7:** Lowpass-filter bandwidth is 22kHz for f = 1kHz and 80kHz for f = 20kHz. Noise floor of test equipment = 10nV/$\sqrt{Hz}$.

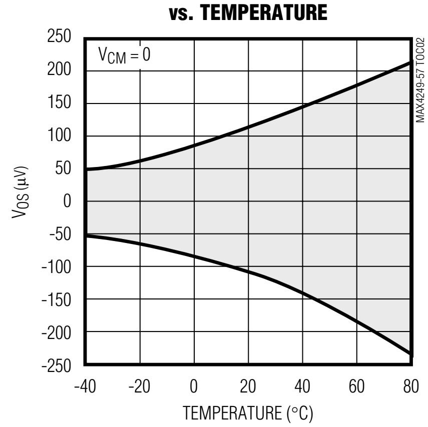
## Typical Operating Characteristics

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = $V_{OUT}$ = $V_{DD}/2$, input noise floor of test equipment =10nV/√Hz for all distortion measurements, $T_A$ = +25°C, unless otherwise noted.)

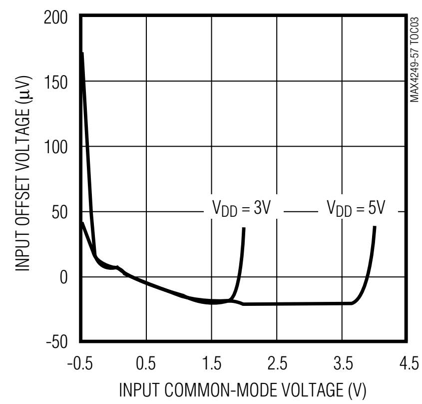
**MAX4251/MAX4256 INPUT OFFSET VOLTAGE DISTRIBUTION**



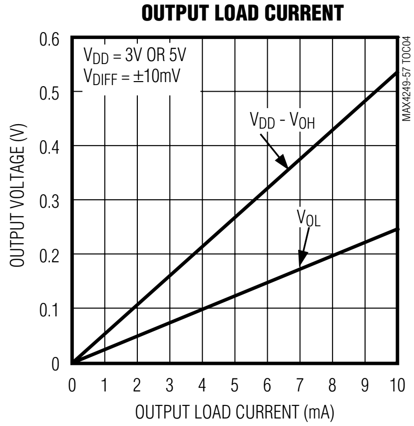

**OFFSET VOLTAGE vs. TEMPERATURE**



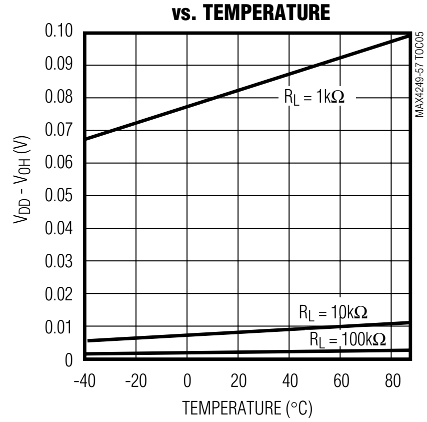

**INPUT OFFSET VOLTAGE vs. INPUT COMMON-MODE VOLTAGE**



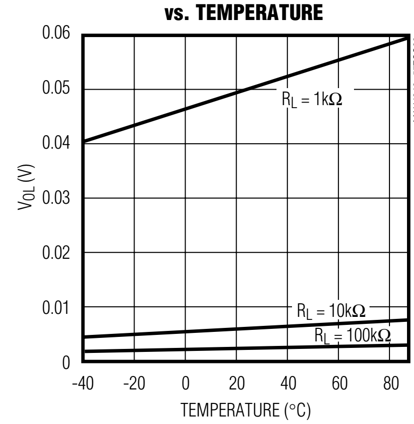

**OUTPUT VOLTAGE vs. OUTPUT LOAD CURRENT**



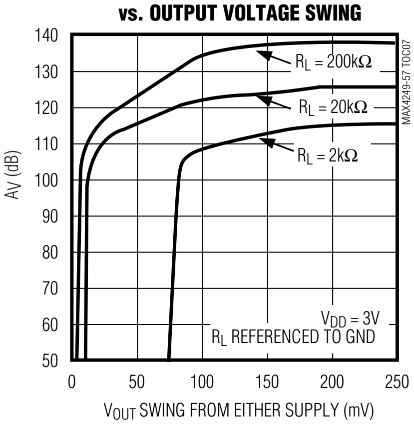

**OUTPUT VOLTAGE SWING ($V_{OH}$) vs. TEMPERATURE**



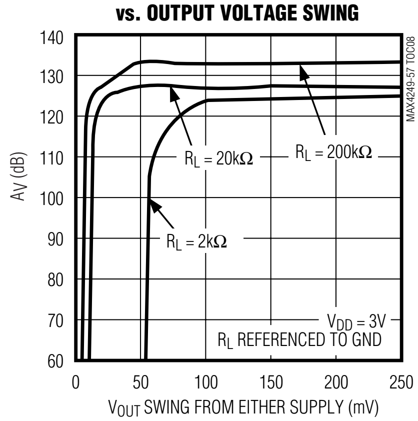

**OUTPUT VOLTAGE SWING ($V_{OL}$) vs. TEMPERATURE**



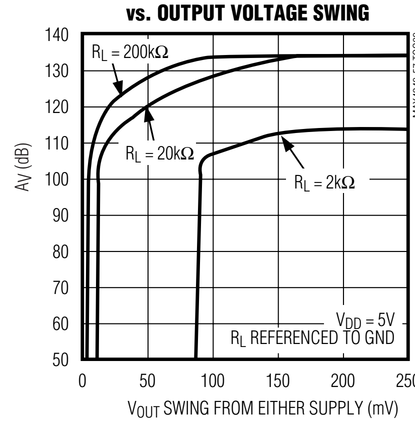

**LARGE-SIGNAL VOLTAGE GAIN vs. OUTPUT VOLTAGE SWING**




**LARGE-SIGNAL VOLTAGE GAIN vs. OUTPUT VOLTAGE SWING**




**LARGE-SIGNAL VOLTAGE GAIN vs. OUTPUT VOLTAGE SWING**

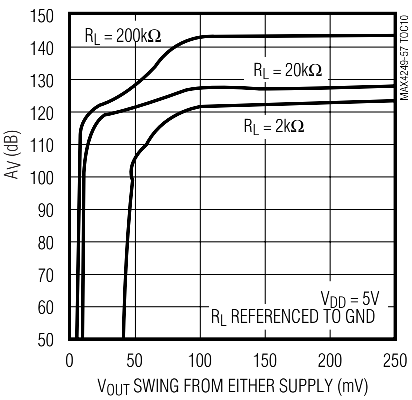


# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

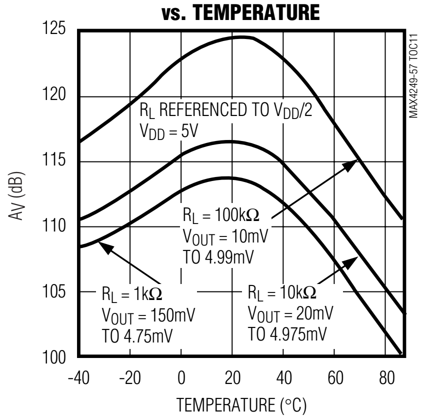
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = $V_{OUT}$ = $V_{DD}/2$, input noise floor of test equipment =10nV/$\sqrt{Hz}$ for all distortion measurements, $T_A$ = +25°C, unless otherwise noted.)

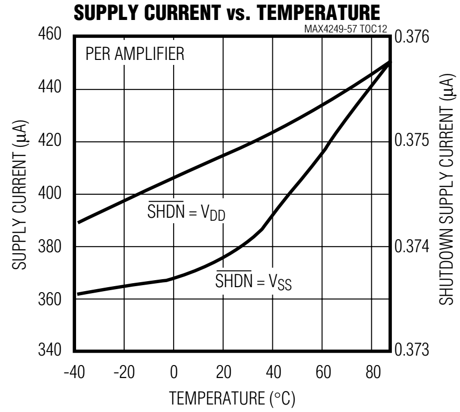
**LARGE-SIGNAL VOLTAGE GAIN vs. OUTPUT VOLTAGE SWING**



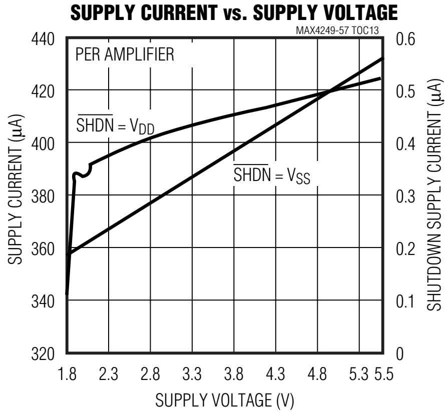

**LARGE-SIGNAL VOLTAGE GAIN vs. TEMPERATURE**



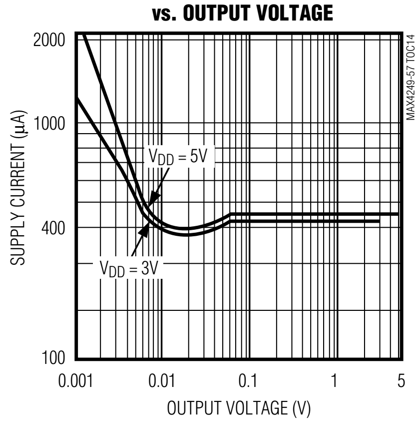

**SUPPLY CURRENT AND SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE**



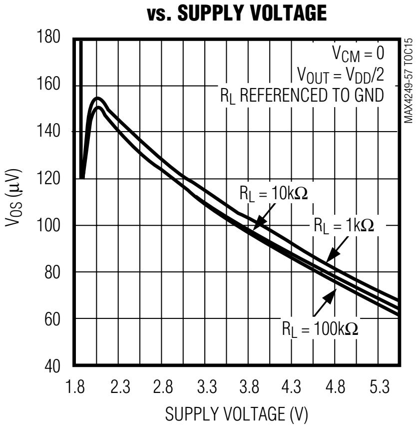

**SUPPLY CURRENT AND SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE**



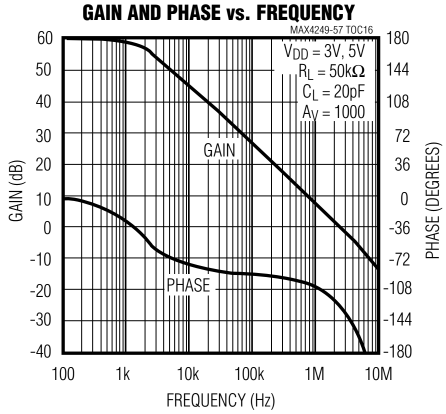

**SUPPLY CURRENT vs. OUTPUT VOLTAGE**



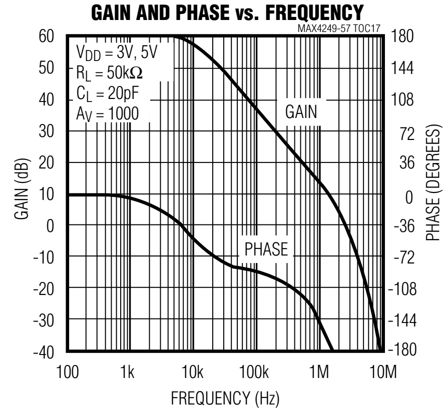

**INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE**



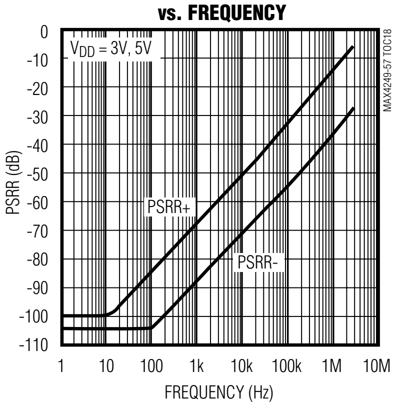

**MAX4250–MAX4254 GAIN AND PHASE vs. FREQUENCY**




**MAX4249/MAX4255/MAX4256/MAX4257 GAIN AND PHASE vs. FREQUENCY**



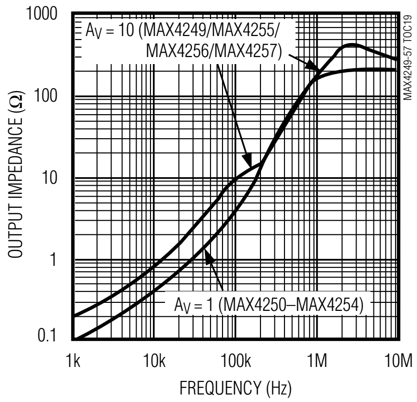

**MAX4250–MAX4254 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY**



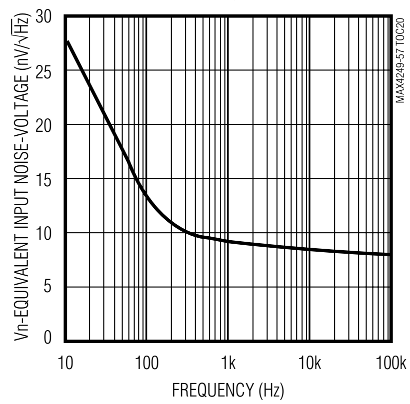
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = $V_{OUT}$ = $V_{DD}$/2, input noise floor of test equipment =10nV/√Hz for all distortion measurements, $T_A$ = +25°C, unless otherwise noted.)

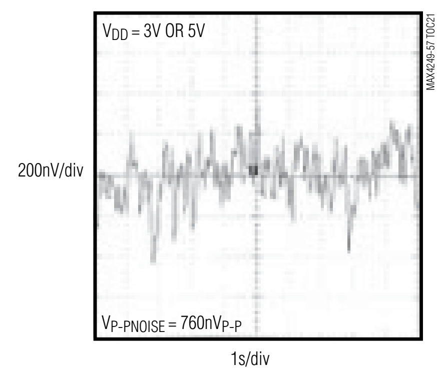
**OUTPUT IMPEDANCE vs. FREQUENCY**



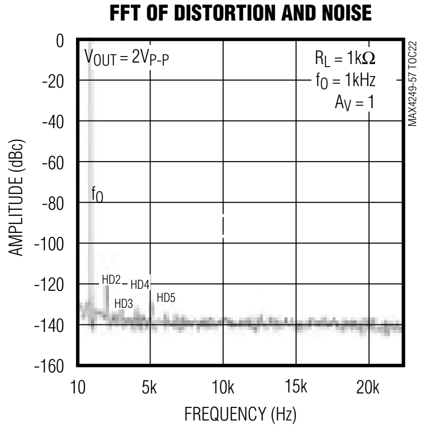

**INPUT VOLTAGE-NOISE DENSITY vs. FREQUENCY**



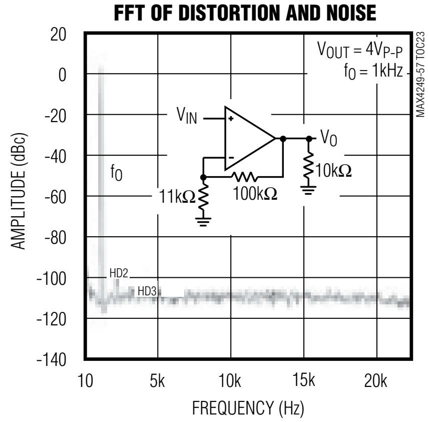

**0.1Hz TO 10Hz P-P NOISE**



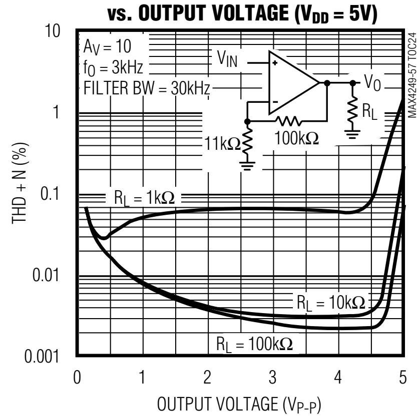

**MAX4250–MAX4254 FFT OF DISTORTION AND NOISE**



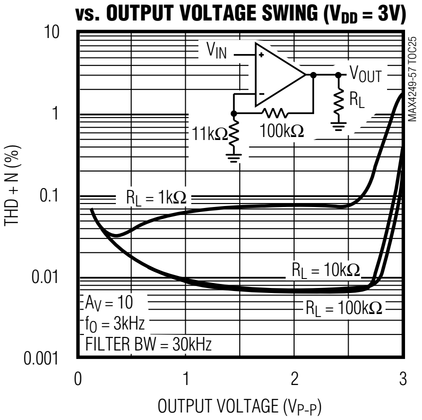

**MAX4249/MAX4255/MAX4256/MAX4257 FFT OF DISTORTION AND NOISE**



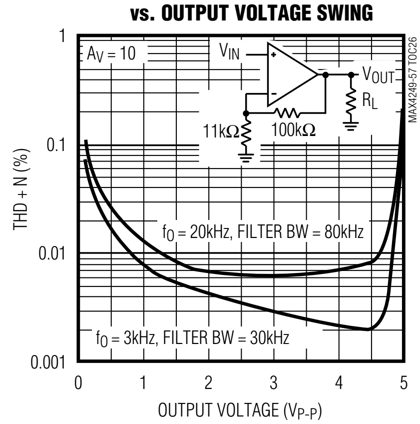

**MAX4250–MAX4254 TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE ($V_{DD}$ = 5V)**



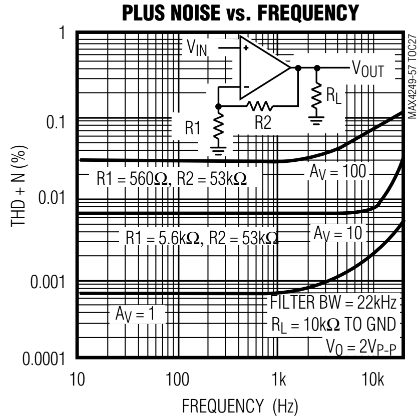

**MAX4250–MAX4254 TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE SWING ($V_{DD}$ = 3V)**




**MAX4249/MAX4255/MAX4256/MAX4257 TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE SWING**




**MAX4250–MAX4254 TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**

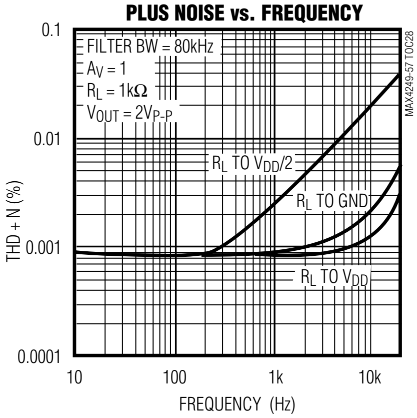


# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

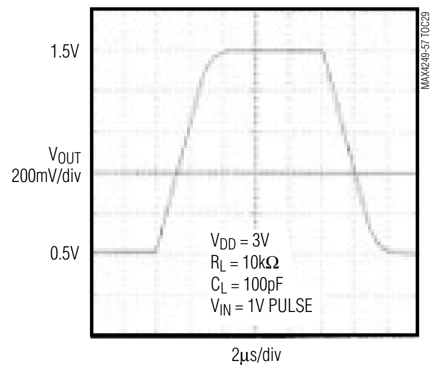
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = $V_{OUT}$ = $V_{DD}/2$, input noise floor of test equipment =10nV/$\sqrt{Hz}$ for all distortion measurements, $T_A$ = +25°C, unless otherwise noted.)

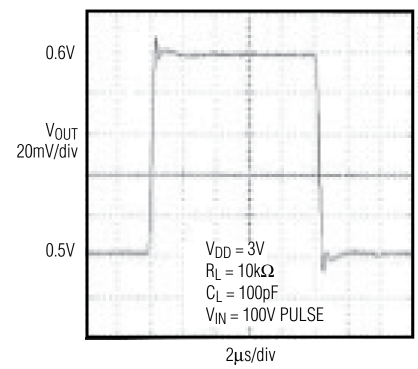
**MAX4250–MAX4254**
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



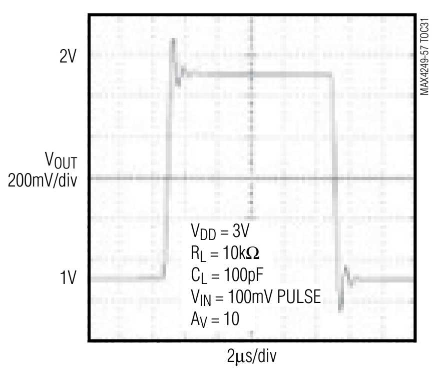

**MAX4250–MAX4254**
**LARGE-SIGNAL PULSE RESPONSE**



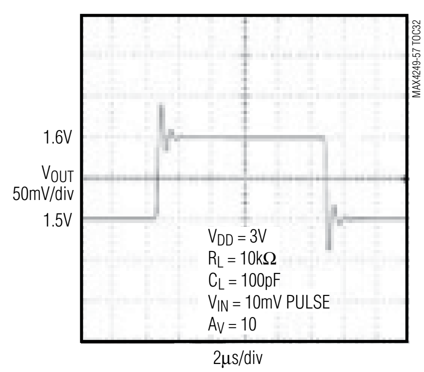

**MAX4250–MAX4254**
**SMALL-SIGNAL PULSE RESPONSE**



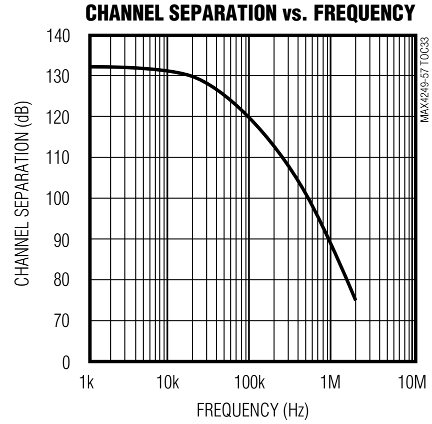

**MAX4249/MAX4255/MAX4256/MAX4257**
**LARGE-SIGNAL PULSE RESPONSE**




**MAX4249/MAX4255/MAX4256/MAX4257**
**SMALL-SIGNAL PULSE RESPONSE**




**CHANNEL SEPARATION vs. FREQUENCY**



## Pin Description

| PIN/BUMP | | | | | | | | NAME | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| MAX4250/ MAX4255 | MAX4251/ MAX4256 | MAX4252/ MAX4257 | MAX4252 | MAX4249/ MAX4253 | | | MAX4254 | | |
| 5-Pin SOT23 | 8-Pin SO/µMAX | 8-Pin SO/µMAX | 8-Pin UCSP | 10-Pin UCSP | 10-Pin µMAX | 14-Pin SO | 14-Pin SO | | |
| 1 | 6 | 1, 7 | A1, A3 | A1, C1 | 1, 9 | 1, 13 | 1, 7, 8, 14 | OUT, OUTA, OUTB, OUTC, OUTD | Amplifier Output |
| 2 | 4 | 4 | C2 | B4 | 4 | 4 | 11 | $V_{SS}$ | Negative Supply. Connect to ground for single-supply operation |
| 3 | 3 | 3, 5 | C1, C3 | A3, C3 | 3, 5 | 3, 11 | 3, 5, 10, 12 | IN+, INA+, INB+, INC+, IND+ | Noninverting Amplifier Input |
| 4 | 2 | 2, 6 | B1, B3 | A2, C2 | 2, 6 | 2, 12 | 2, 6, 9, 13 | IN-, INA-, INB-, INC-, IND- | Inverting Amplifier Input |
| 5 | 7 | 8 | A2 | B1 | 8 | 14 | 4 | $V_{DD}$ | Positive Supply |
| — | 8 | — | — | A4, C4 | — | 5, 9 | — | $\overline{SHDN}$, $\overline{SHDNA}$, $\overline{SHDNB}$ | Shutdown Input, Connect to $V_{DD}$ or leave unconnected for normal operation (amplifier(s) enabled). |
| — | 1, 5 | — | — | — | — | 5, 7, 8, 10 | — | N.C. | No Connection. Not internally connected. |
| — | — | — | B2 | B2, B3 | — | — | — | — | Not populated with solder sphere |

## Detailed Description

The MAX4249–MAX4257 single-supply operational amplifiers feature ultra-low noise and distortion while consuming very little power. Their low distortion and low noise make them ideal for use as preamplifiers in wide dynamic-range applications, such as 16-bit analog-to-digital converters (see *Typical Operating Circuit*). Their high-input impedance and low noise are also useful for signal conditioning of high-impedance sources, such as piezoelectric transducers.

These devices have true rail-to-rail ouput operation, drive loads as low as 1kΩ while maintining DC accuracy, and can drive capactive loads up to 400pF without oscillation. The input common-mode voltage range extends from $V_{DD}$ - 1.1V to 200mV beyond the negative rail. The push-pull output stage maintains excellent DC characteristics, while delivering up to ±5mA of current.

The MAX4250–4254 are unity-gain stable, whereas, the MAX4249/MAX4255/MAX4256/MAX4257 have a higher slew rate and are stable for gains ≥ 10V/V. The MAX4249/MAX4251/MAX4253/MAX4256 feature a low-power shutdown mode, which reduces the supply current to 0.5µA and disables the outputs.

### Low Distortion

Many factors can affect the noise and distortion that the device contributes to the input signal. The following guidelines offer valuable information on the impact of design choices on Total Harmonic Distortion (THD).

Choosing proper feedback and gain resistor values for a particular application can be a very important factor in reducing THD. In general, the smaller the closed-loop gain, the smaller the THD generated, especially when driving heavy resistive loads. Large-value feedback resistors can significantly improve distortion. The THD of the part normally increases at approximately 20dB per decade, as a function of frequency. Operating the device near or above the full-power bandwidth significantly degrades distortion.

Referencing the load to either supply also improves the part's distortion performance, because only one of the MOSFETs of the push-pull output stage drives the output. Referencing the load to midsupply increases the part's distortion for a given load and feedback setting. (See the Total Harmonic Distortion vs. Frequency graph in the *Typical Operating Characteristics*.)

For gains ≥ 10V/V, the decompensated devices MAX4249/MAX4255/MAX4256/MAX4257 deliver the best distortion performance, since they have a higher slew rate and provide a higher amount of loop gain for a given closed-loop gain setting. Capacitive loads below 400pF, do not significantly affect distortion results. Distortion performance remains relatively constant over supply voltages.

### Low Noise

The amplifier's input-referred, noise-voltage density is dominated by flicker noise at lower frequencies, and by thermal noise at higher frequencies. Because the thermal noise contribution is affected by the parallel combination of the feedback resistive network ($R_F \parallel R_G$, Figure 1), these resistors should be reduced in cases where the system bandwidth is large and thermal noise is dominant. This noise contribution factor decreases, however, with increasing gain settings.

For example, the input noise-voltage density of the circuit with $R_F$ = 100kΩ, $R_G$ = 11kΩ ($A_V$ = 10V/V) is $e_n$ = 15nV/√Hz, $e_n$ can be reduced to 9nV/√Hz by choosing $R_F$ = 10kΩ, $R_G$ = 1.1kΩ ($A_V$ = 10V/V), at the expense of greater current consumption and potentially higher distortion. For a gain of 100V/V with $R_F$ = 100kΩ, $R_G$ = 1.1kΩ, the $e_n$ is low (9nV/√Hz).

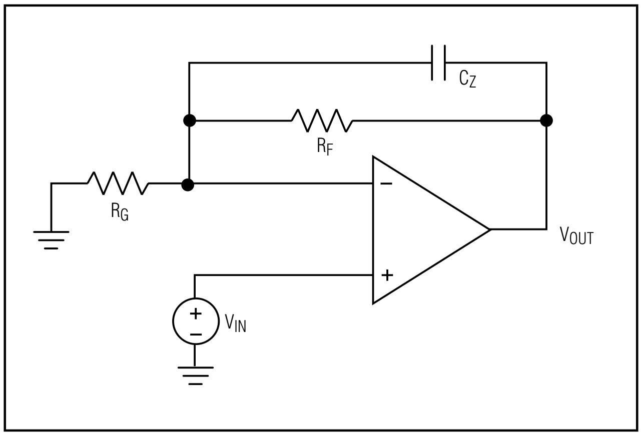



*Figure 1. Adding Feed-Forward Compensation*

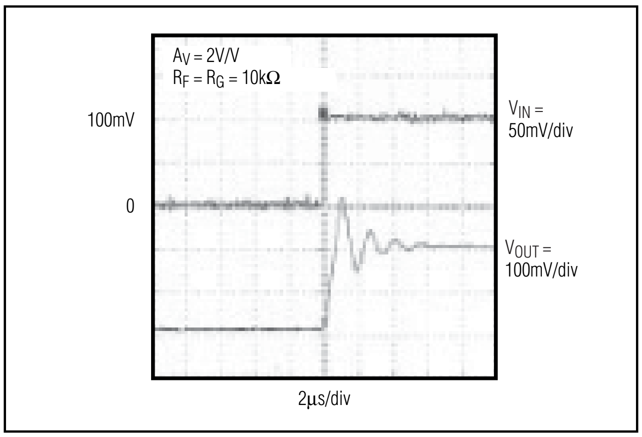



*Figure 2a. Pulse Response with No Feed-Forward Compensation*

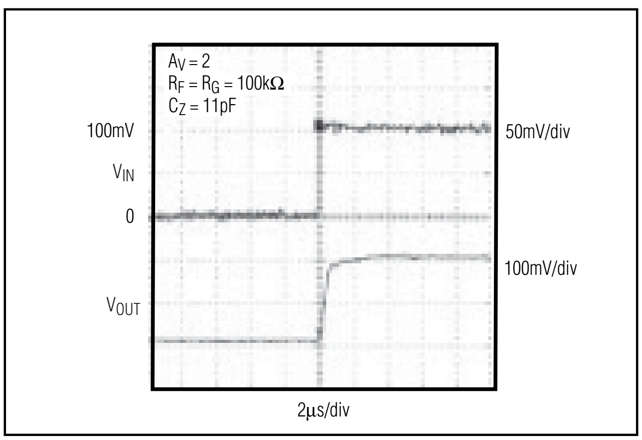



*Figure 2b. Pulse Response with 10pF Feed-Forward Compensation*

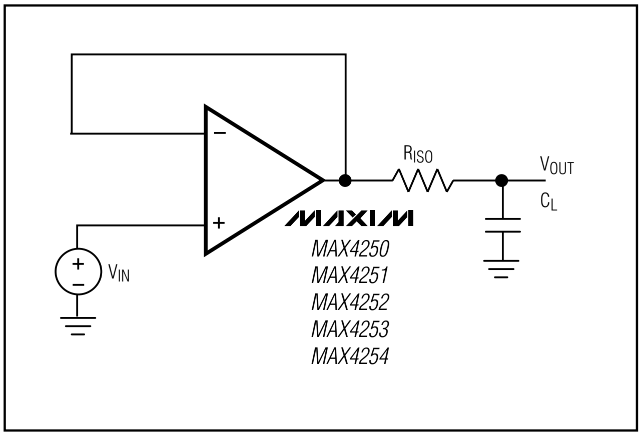



*Figure 3. Overdriven Input Showing No Phase Reversal*

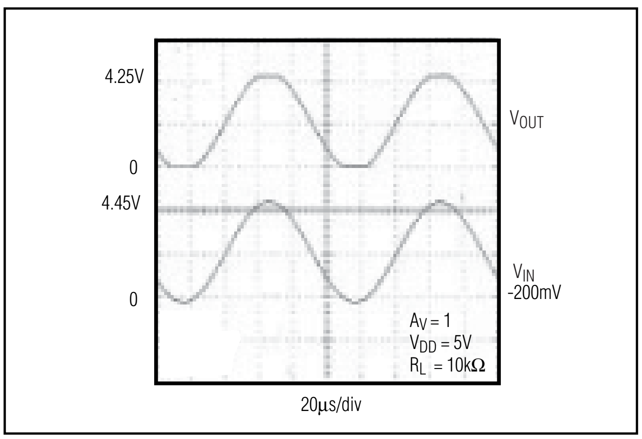



*Figure 4. Rail-to-Rail Output Operation*

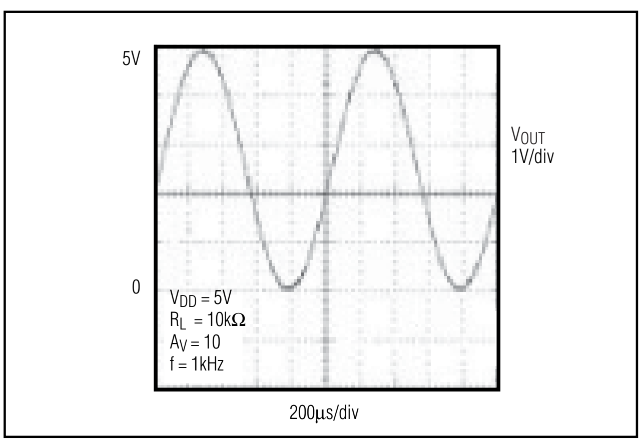



*Figure 5. Capacitive-Load Driving Circuit*

### *Using a Feed-Forward Compensation Capacitor, $C_Z$*

The amplifier's input capacitance is 11pF. If the resistance seen by the inverting input is large (feedback network), this can introduce a pole within the amplifier's bandwidth, resulting in reduced phase margin. Compensate the reduced phase margin by introducing a feed-forward capacitor ($C_Z$) between the inverting input and the output (Figure 1). This effectively cancels the pole from the inverting input of the amplifier. Choose the value of $C_Z$ as follows:

$$C_Z = 11 \times (R_F / R_G) \text{ [pF]}$$

In the unity-gain stable MAX4250–MAX4254, the use of a proper $C_Z$ is most important for $A_V$ = 2V/V, and $A_V$ = -1V/V. In the decompensated MAX4249/MAX4255 /MAX4256/MAX4257, $C_Z$ is most important for $A_V$ = 10V/V. Figures 2a and 2b show transient response both with and without $C_Z$.

Using a slightly smaller $C_Z$ than suggested by the formula above achieves a higher bandwidth at the expense of reduced phase and gain margin. As a general guideline, consider using $C_Z$ for cases where $R_G$ II $R_F$ is greater than 20kΩ (MAX4250–MAX4254) or greater than 5kΩ (MAX4249/MAX4255/MAX4256/ MAX4257).

## *Applications Information*

The MAX4249–MAX4257 combine good driving capability with ground-sensing input and rail-to-rail output operation. With their low distortion, low noise and low-power consumption, these devices are ideal for use in portable instrumentation systems and other low-power, noise-sensitive applications.

### *Ground-Sensing and Rail-to-Rail Outputs*

The common-mode input range of these devices extends below ground, and offers excellent common-mode rejection. These devices are guaranteed not to undergo phase reversal when the input is overdriven (Figure 3).

Figure 4 showcases the true rail-to-rail output operation of the amplifier, configured with $A_V$ = 10V/V. The output swings to within 8mV of the supplies with a 10kΩ load, making the devices ideal in low-supply-voltage applications.

### *Output Loading and Stability*

Even with their low quiescent current of 400µA, these amplifiers can drive 1kΩ loads while maintaining excellent DC accuracy. Stability while driving heavy capacitive loads is another key feature.

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

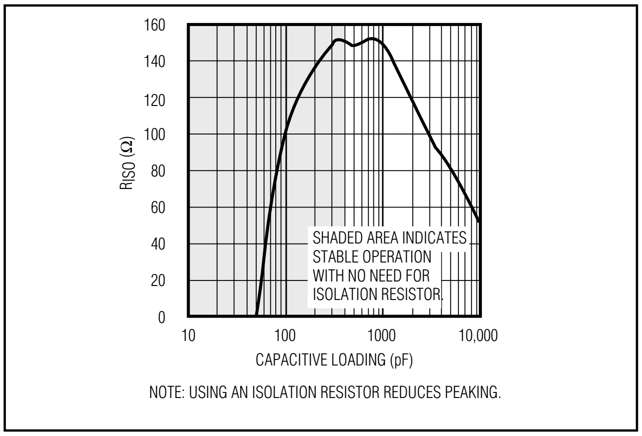



*Figure 6. Isolation Resistance vs. Capacitive Loading to Minimize Peaking (<2dB)*

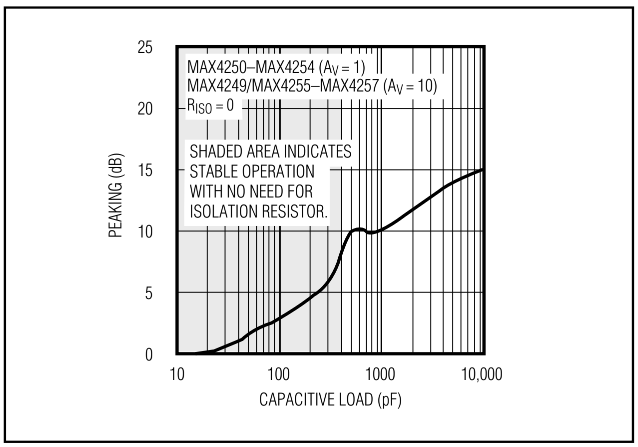



*Figure 7. Peaking vs. Capacitive Load*

These devices maintain stability while driving loads up to 400pF. To drive higher capacitive loads, place a small isolation resistor in series between the output of the amplifier and the capacitive load (Figure 5). This resistor improves the amplifier's phase margin by isolating the capacitor from the op amp's output. Reference Figure 6 to select a resistance value that will ensure a load capacitance that limits peaking to <2dB (25%). For example, if the capacitive load is 1000pF, the corresponding isolation resistor is 150Ω. Figure 7 shows that peaking occurs without the isolation resistor. Figure 8 shows the unity-gain bandwidth vs. capacitive load for the MAX4250–MAX4254.

### Power Supplies and Layout

The MAX4249–MAX4257 operate from a single 2.4V to 5.5V power supply or from dual supplies of ±1.20V to ±2.75V. For single-supply operation, bypass the power

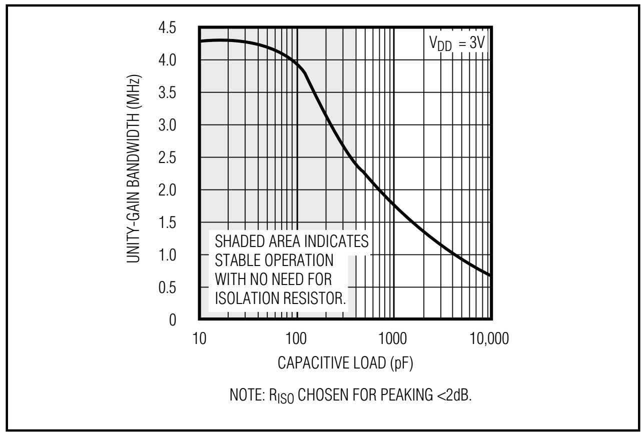



*Figure 8. MAX4250-4254 Unity-Gain Bandwidth vs. Capacitive Load*

supply with a 0.1µF ceramic capacitor placed close to the $V_{DD}$ pin. If operating from dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and output. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components close to the op amp's pins.

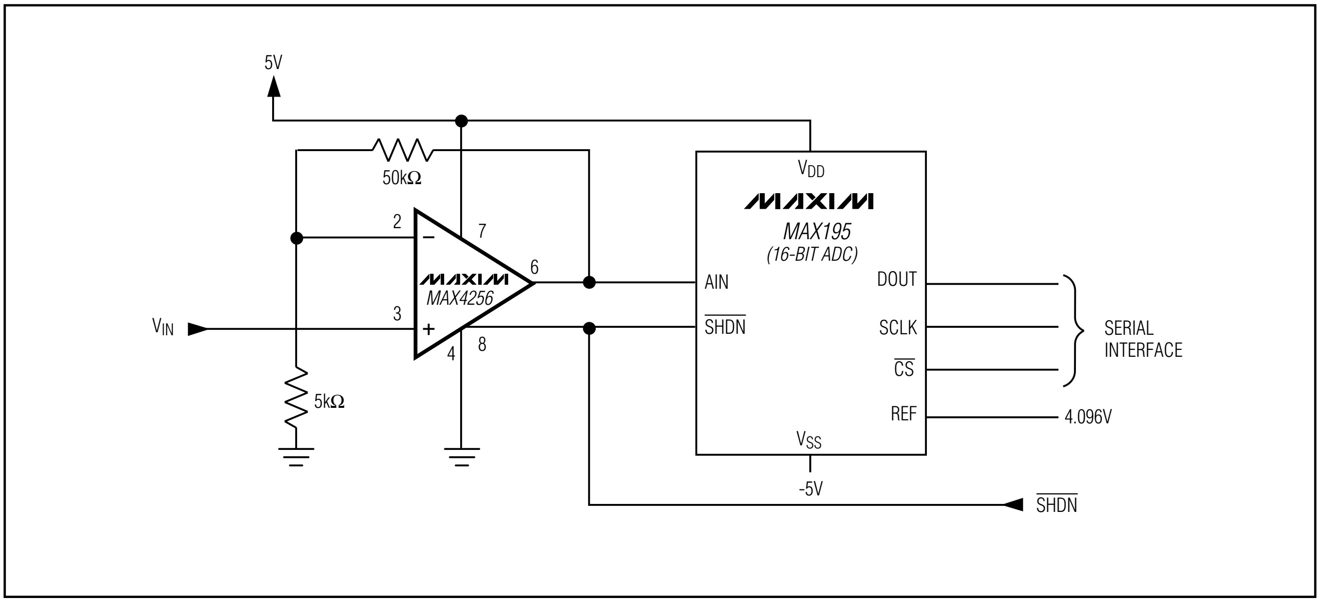
### UCSP Package Consideration

For general UCSP package information and PC layout considerations, please refer to the Maxim Application Note (Wafer-Level Ultra-Chip-Board-Scale-Package).

## UCSP Reliability

The UCSP represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP. Performance through operating life test and moisture resistance remains uncompromised as it is primarily determined by the wafer-fabrication process. Mechanical stress performance is a greater consideration for a UCSP. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder-joint contact integrity must be considered. Table 1 shows the testing done to characterize the UCSP reliability performance. In conclusion, the UCSP is capable of performing reliably through environmental stresses as indicated by the results in the table. Additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com.

## Typical Operating Circuit




## Table 1. Reliability Test Data

| TEST | CONDITIONS | DURATION | NO. OF FAILURES PER SAMPLE SIZE |
|---|---|---|---|
| Temperature Cycle | -35°C to +85°C, -40°C to +100°C | 150 cycles, 900 cycles | 0/10, 0/200 |
| Operating Life | $T_A$ = +70°C | 240h | 0/10 |
| Moisture Resistance | -20°C to +60°C, 90% RH | 240h | 0/10 |
| Low-Temperature Storage | -20°C | 240h | 0/10 |
| Low-Temperature Operational | -10°C | 24h | 0/10 |
| Solderability | 8h steam age | — | 0/15 |
| ESD | ±2000V, Human Body Model | — | 0/5 |
| High-Temperature Operating Life | $T_J$ = +150°C | 168h | 0/45 |

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Selector Guide

| PART | GAIN BANDWIDTH (MHz) | MINIMUM STABLE GAIN (V/V) | NO. OF AMPLIFIERS PER PACKAGE | SHUTDOWN MODE | PIN-PACKAGE |
|---|---|---|---|---|---|
| MAX4249 | 22 | 10 | 2 | Yes | 10-pin µMAX, 14-pin SO |
| MAX4250 | 3 | 1 | 1 | — | 5-pin SOT23 |
| MAX4251 | 3 | 1 | 1 | Yes | 8-pin µMAX/SO |
| MAX4252 | 3 | 1 | 2 | — | 8-pin µMAX/SO, 8-pin UCSP |
| MAX4253 | 3 | 1 | 2 | Yes | 10-pin µMAX, 14-pin SO, 10-pin UCSP |
| MAX4254 | 3 | 1 | 4 | — | 14-pin SO |
| MAX4255 | 22 | 10 | 1 | — | 5-pin SOT23 |
| MAX4256 | 22 | 10 | 1 | Yes | 8-pin µMAX/SO |
| MAX4257 | 22 | 10 | 2 | — | 8-pin µMAX/SO |

## Ordering Information (continued)

| PART | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|---|---|---|---|
| **MAX4251**ESA | -40°C to +85°C | 8 SO | — |
| MAX4251EUA | -40°C to +85°C | 8µMAX | — |
| **MAX4252**EBL-T* | -40°C to +85°C | 8 UCSP-8 | AAO |
| MAX4252ESA | -40°C to +85°C | 8 SO | — |
| MAX4252EUA | -40°C to +85°C | 8 µMAX | — |
| **MAX4253**EBC-T* | -40°C to +85°C | 10 UCSP-10 | AAK |
| MAX4253EUB | -40°C to +85°C | 10 µMAX | — |
| MAX4253ESD | -40°C to +85°C | 14 SO | — |
| **MAX4254**ESD | -40°C to +85°C | 14 SO | — |
| **MAX4255**EUK-T | -40°C to +85°C | 5 SOT23-5 | ACCJ |
| **MAX4256**ESA | -40°C to +85°C | 8 SO | — |
| MAX4256EUA | -40°C to +85°C | 8 µMAX | — |
| **MAX4257**ESA | -40°C to +85°C | 8 SO | — |
| MAX4257EUA | -40°C to +85°C | 8 µMAX | — |

**UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. Refer to the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.*

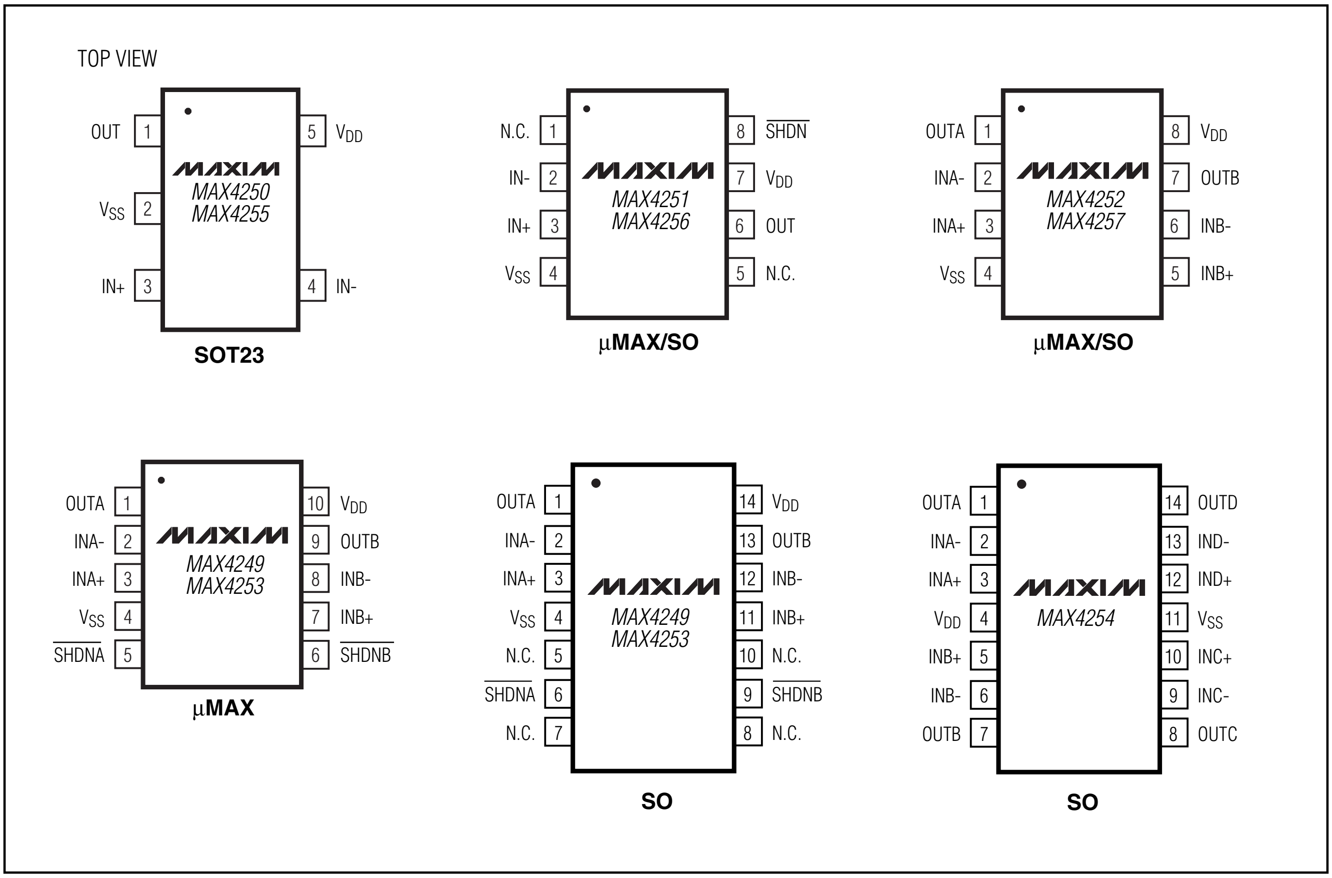
## Chip Information

MAX4250/MAX4251/MAX4255/MAX4256 TRANSISTOR COUNT: 170

MAX4249/MAX4252/MAX4253/MAX4257 TRANSISTOR COUNT: 340

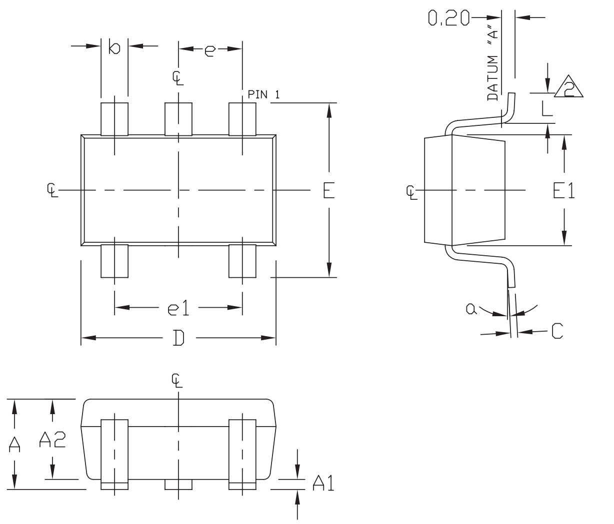
MAX4254 TRANSISTOR COUNT: 680

## Pin Configurations (continued)



## Package Information

SOT5L.EPS

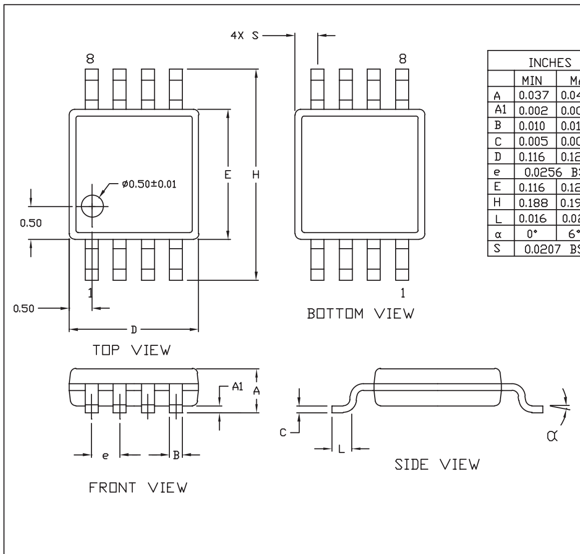



| SYMBOL | MIN | MAX |
|---|---|---|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.35 | 0.50 |
| C | 0.08 | 0.20 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.35 | 0.55 |
| e | 0.95 REF | |
| e1 | 1.90 REF | |
| α | 0° | 10° |

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. MEETS JEDEC MO178.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SOT-23, 5L
APPROVAL | DOCUMENT CONTROL NO. 21-0057 | REV C | 1/1

8LUMAXD.EPS



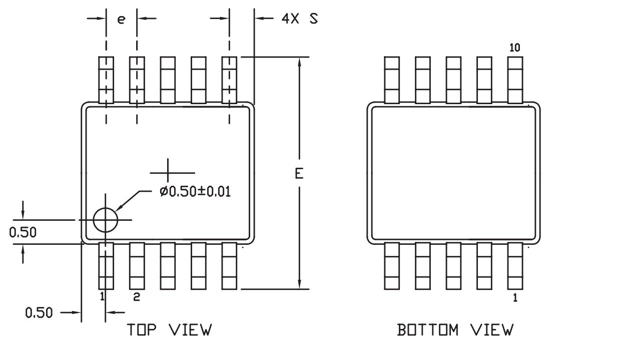

| | INCHES | | MILLIMETERS | | JEDEC INCHES | | JEDEC MILLIMETERS | |
|---|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| A | 0.037 | 0.043 | 0.94 | 1.10 | --- | 0.043 | --- | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 |
| B | 0.010 | 0.014 | 0.25 | 0.36 | 0.010 | 0.016 | 0.25 | 0.40 |
| C | 0.005 | 0.007 | 0.13 | 0.18 | 0.005 | 0.009 | 0.13 | 0.23 |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 0.114 | 0.122 | 2.9 | 3.1 |
| e | 0.0256 BSC | | 0.65 BSC | | 0.0256 BSC | | 0.64 BSC | |
| E | 0.116 | 0.120 | 2.95 | 3.05 | 0.114 | 0.122 | 2.9 | 3.1 |
| H | 0.188 | 0.198 | 4.78 | 5.03 | 0.193 BSC | | 4.9 BSC | |
| L | 0.016 | 0.026 | 0.41 | 0.66 | 0.016 | 0.027 | 0.40 | 0.70 |
| α | 0° | 6° | 0° | 6° | 0° | 6° | 0° | 6° |
| S | 0.0207 BSC | | 0.5250 BSC | | | | | |

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.

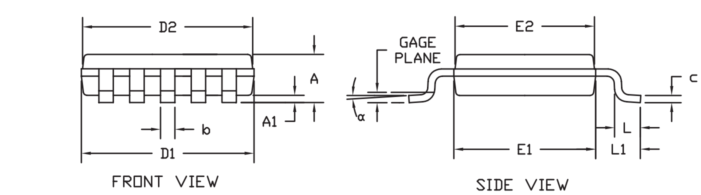
MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 8L uMAX
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV I | 1/1

## Package Information (continued)

10LUMAX.EPS




| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.037 | 0.043 | 0.94 | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| D1 | 0.116 | 0.120 | 2.95 | 3.05 |
| D2 | 0.114 | 0.118 | 2.89 | 3.00 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 |
| E2 | 0.114 | 0.118 | 2.89 | 3.00 |
| E | 0.187 | 0.199 | 4.75 | 5.05 |
| L | 0.0157 | 0.0275 | 0.40 | 0.70 |
| L1 | 0.037 REF | | 0.940 REF | |
| b | 0.007 | 0.0106 | 0.177 | 0.270 |
| e | 0.0197 BSC | | .500 BSC | |
| c | 0.0035 | 0.0078 | 0.090 | 0.200 |
| S | 0.0196 REF | | .498 REF | |
| α | 0° | 6° | 0° | 6° |



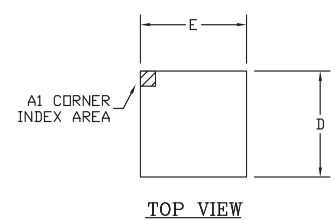

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO187.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 10L uMAX
APPROVAL | DOCUMENT CONTROL NO. 21-0061 | REV H | 1/1

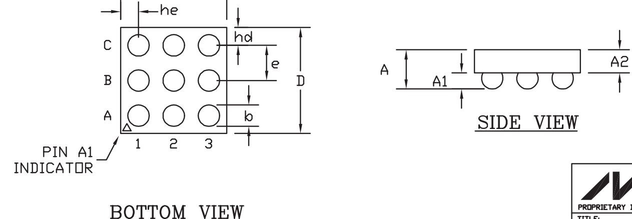
9LUCSP, 3x3.EPS

| SYMBOL | DIMENSIONS |
|---|---|
| A | 0.60±0.05 |
| D | 1.52±0.05 |
| E | 1.52±0.05 |
| e | 0.50 BASIC |
| b | ø 0.35 BASIC |
| A1 | 0.27±0.04 |
| A2 | 0.33 Ref. |
| hd | 0.26 Ref. |
| he | 0.26 Ref. |

| SOLDER BALL DEPOPULATION | |
|---|---|
| PKG. CODE | DEPOPULATED BALL |
| B9-1 | NONE |
| B9-2 | B2 |
| B9-3 | B1, B2, B3 |




NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MEETS JEDEC M0195.

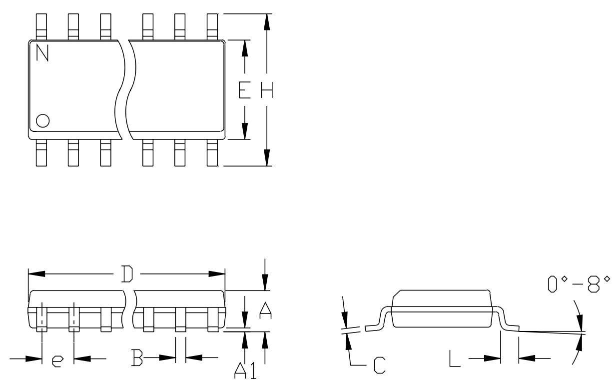



MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 3x3 UCSP
APPROVAL | DOCUMENT CONTROL NO. 21-0093 | REV. E | 1/1

# UCSP, Single-Supply, Low-Noise, Low-Distortion, Rail-to-Rail Op Amps

## Package Information (continued)

SOICN.EPS




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 | | 1.27 | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| h | 0.010 | 0.020 | 0.25 | 0.50 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N | MS012 |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | A |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | B |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | C |

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

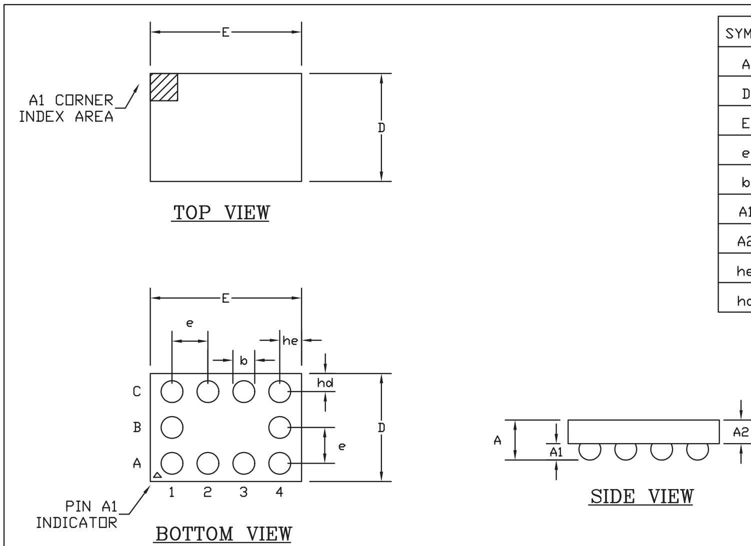
MAXIM
120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: SOIC .150"

1/1

DOCUMENT CONTROL NUMBER: 21-0041 REV: A

## Package Information (continued)




| SYMBOL | DIMENSIONS |
|---|---|
| A | 0.022 ±.002 |
| D | 0.059 ±.002 |
| E | 0.084 ±.002 |
| e | 0.0197 BASIC |
| b | ø 0.0120 BASIC |
| A1 | 0.009±.0015 |
| A2 | 0.013 Ref. |
| he | 0.012 Ref. |
| hd | 0.010 Ref. |

12L, USPC.EPS

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. MEETS JEDEC MO195.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 12L UCSP, 4x3 (B12-4), PY72

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0099 | C | 1/1 |